

Docket No.: 60409.300903

Patent

REMARKS

The Examiner is thanked for the comments in the Action. They have helped us considerably in understanding the Action and in drafting this Response thereto. It is our understanding that claims 1-26 remain pending in this application.

Item 1 (Claim Objections):

The Actions here states:

Applicant is advised that should claims 1-13 be found allowable, claims 14-26 will be objected to under 37 CFR 1.75 as being a substantial duplicate thereof. When two claims in an application are duplicates or else are so close in content that they both cover the same thing, despite a slight difference in wording, it is proper after allowing one claim to object to the other as being a substantial duplicate of the allowed claim. See MPEP § 706.03(k).

Respectfully this is error. MPEP § 706.03(k) states that “*court decisions have confirmed applicant's right to restate (i.e., by plural claiming) the invention in a reasonable number of ways. Indeed, a mere difference in scope between claims has been held to be enough.*” Here claims 1-13 are general apparatus type claims reciting specific elements. In contrast, claims 14-26 are means-plus-function type claims and have a different scope than claims 1-13 as a matter of law (35 U.S.C. 112, 6th paragraph). Congress specifically included means-plus-function claims in the 1952 Patent Act and the courts, including the U.S. Supreme Court, have upheld them as having a different scope than non-means-plus-function type claims. We accordingly ask the Examiner to reconsider.

Item 2 (§112 ¶2 rejections):

Claims 1-13, 17, and 23 are rejected as indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

The Actions here states “*Regarding claims 4, 10, 17, 23 the phrase “potential” renders the claim indefinite because it is unclear whether the limitation(s) following the phrase merely have the potential to do so or actually do so.*”

Responsive hereto, applicant has amended claims 4, 10, 17, and 23.

The Actions continues, “*Regarding claims 1, 3, 4, 5, 6, 8, 9, 10, 11, 12 the phrase “able to” renders the claim indefinite because it is unclear what “able to” comprises.*”

Responsive hereto, applicant has amended claims 1, 3, 4, 5, 6, 8, 9, 10, 11, and 12.

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The Actions continues, "*Claim 4 recites the limitation "said hash value" in line 2. There is insufficient antecedent basis for this limitation in the claim.*"

Responsive hereto, applicant has amended claim 4.

No new subject matter is added by any of these amendments.

Item 3 (§ 102(b) rejections):

Claims 1-5 and 14-18 are rejected as being anticipated by Tamura. Respectfully this is error.

Regarding claim 1, the Action here states "*Tamura teaches, "A search engine, comprising: -- a controller able to provide a search value representing a search result [Figure 4, item Control Unit, Column 4, lines 24-42]."*" We urge that it will become clear as we proceed that Tamura's control unit 606 is inherently not equivalent to Applicant's controller 212. Our point now is that this has Tamura's 62-bit wide packet (FIG. 2 and col. 4, ln. 32-33) being regarded as equivalent to Applicant's search value. As will also become clear, this distinguishes the two inventions.

The Action next states (that Tamura teaches) "*-- a memory able to store a search database of said search results and to provide instances of said search results to said controller [Figure 4, item 611, Column 4, lines 24-42]."* However, FIG. 4 clearly shows and the text clearly states (e.g., col. 4, ln. 31) that item 611 is a FIFO memory. As is well known in the art, "FIFO" means first-in-first-out and a FIFO memory is a particular form of memory that cannot be addressably accessed. In contrast, Applicant's claim 1 is directed to a "*search engine*" and recites "*a memory able to store a search database of said search results and to provide instances of said search results to said controller.*" One of ordinary skill in the art will readily appreciate that a FIFO memory is unsuitable to store a search engine database that necessarily is addressably accessed. Accordingly, Applicant's memory is a major claim element that is not taught or reasonably suggested by the prior art.

The Action next states (that Tamura teaches) "*-- a hash-CAM sub-circuit (H-CAM) including ... a hash unit able to receive said search value from said controller and generate a hash output based there on [Figure 4, item 601]."* However, in good conscience, we respectfully point out that Tamura's hash memory 601 is wrongly interpreted. It is a 41x512 memory (FIG. 6, col. 56-58), rather than a hash function calculator as relied on to support the rejection. Rather, in

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Tamura its address generator 101 is its hash function calculator (col. 4, ln. 39-42), and this cannot be reconciled with the claimed invention.

Tamura's address generator 101 receives two 9-bit portions of its 62-bit wide packet, and generates a 9-bit hash address (see e.g., FIG. 5). In contrast, the hash unit in Applicant's claim 1 receives its search value – not merely two small portions of it. Accordingly, Applicant's hash unit is another major claim element that is not taught or reasonably suggested by the prior art.

The Action next states (that Tamura's alleged H-CAM includes) "*a CAM unit [Figure 4, item 602] able to store a CAM database of instances of said search values known to cause hash collisions in said hash unit [Column 3, lines 37-47],...*" However, Tamura's associative memory 602 also cannot be reconciled with the claimed invention.

FIG. 7 shows and col. 5, ln. 5 through col. 7, ln. 4 state details of Tamura's somewhat mislabeled associative memory 602. In particular, this element actually includes a CAM 201 and a RAM 202. The CAM 201 receives the 31-bit wide "identifier" field and the RAM 202 receives the 18-bit operand data (OD) field from its 62-bit wide packet (see also, col. 4, ln. 50-52). But the 31-bit identifier that actually is used with CAM-type memory is here again only a portion of what is apparently relied on as being equivalent to Applicant's search value. Note also, that this 31-bit identifier is not the same as the two 9-bit portions of its 62-bit wide packet that are received by its address generator 101. In contrast, in Applicant's claim 1 both the hash unit and the CAM unit receive the same search value. Accordingly, Applicant's CAM unit is another major claim element that is not taught or reasonably suggested by the prior art.

Continuing on this, the Action states (that Tamura's alleged CAM unit is) "... *to receive said search value from said controller [Column 4, lines 43-49],...*" but we have just shown that this is incorrect. Then the Action states "... *and to match said search value against said CAM database such that a CAM output is provided if a match exists [Column 5, lines 5-36].*" However, the output (hash address) of Tamura's address generator 101 is 9-bits wide; the output (read data) of its hash memory 601 is 40-bits (arguably actually 41); and that of its associative memory 602 is 50-bits wide, wherein 32-bits (31+1) come from that unit's CAM 201 and the other 18-bits come from its RAM 202.

With all of the above as ground work, we can argue points of distinction between Tamura's control unit 606 and Applicant's controller and Tamura's items 605 and 603 and Applicant's logic unit, but we respectfully submit that such would be redundant. We have shown

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that a number of major claim elements here are not taught or reasonably suggested by the prior art.

Regarding claims 2-5 and 14-18, generally, we urge that these are allowable for at least the reasons stated above.

Regarding claim 2 further, the Action states "*Tamura teaches the search engine of claim 1, 'wherein said hash unit is programmable to employ different hash algorithms [Column 12, lines 52- 56]' as claimed.*" Respectfully this is further error. The Action posits that Tamura's hash memory 601 is equivalent a hash function calculator. As we have shown already, this hash memory 601 is simply memory, and as such is not "*programmable to employ different hash algorithms*" to calculate anything. As for Tamura's address generator 101, which is a hash function calculator, this is not programmable. First, we can find no clear support for such in the cited portion of Tamura. FIG. 4, especially FIG. 5, and the text all clearly indicate that Tamura's address generator 101 is a simple exclusive-OR unit. The "Normal" and "Bit Reverse" calculations discussed in the cited portion of Tamura are not achieved by putting the same data through a different algorithm. They are achieved by changing the ordering of the data and putting it through the same algorithm.

Regarding claim 4 further, the Action states "*Tamura teaches the search engine of claim 1, 'wherein ... said H-CAM further includes: -- a search data storage [Figure 4, item 611] able to store a plurality of hash pointer values and a plurality of search data values,....'*" However, the FIFO memory 611 has already been relied on as being (wrongly) equivalent to Applicant's memory in claim 1. Is the Action asserting that the FIFO memory 611 of Tamura is fulfilling two equivalencies to the claimed invention? We urge not.

In any case, a FIFO memory is a particular form of memory that one of ordinary skill in the art will readily appreciate, here as well, is one unsuitable to store and handle data as recited in claim 4.

Item 4 (§ 103(a) rejections):

As an initial point, the Action states "*the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary.*" This presumption is correct.

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Claims 6-13 and 19-26 are rejected as being unpatentable (obvious) over Tamura. Respectfully this is error.

The Action here states:

Claims 6-13 are considered to be mere duplication of parts of claims 1-5 and therefore obvious and thus are rejected with the art applied to claims 1-5 and in light of In re Harza, 274 F.2d 669, 124 USPQ 378 (CCPA 1960). Claims containing limitations with duplication of parts have no patentable significance unless a new and unexpected result is produced.

Regarding claim 6-13, the Applicant fails to show how the duplication of parts present in claims 6-13 produce a new and unexpected result over claims 1-5 or the prior art.

As a first point in rebuttal, this rejection necessarily fails if the rejection of claim 1 fails. We urge that this is the case, and that these claims are therefore also allowable for at least the reasons stated above.

Next, we urge that the claimed invent is distinguishable under the rationale of the cited case and the standard it is cited in support of. In Harza, the duplication was literal duplication. In contrast, in claims 6-13 this is not so. The sequentially paired hash units and CAM units in Applicant's claims each receive decreasingly smaller input values and provide decreasingly smaller output values. This can be seen in Applicant's FIGS. 5-7 and TBL. 2, as discussed in the specification at paragraphs [0065]-[0104], and this is implicit in the claims by the inherent nature of a hash calculation or a circuit that performs such.

As for the new and unexpected result that is produced, the improvement of a two-level H-CAM (e.g., FIG. 4) is not merely the ability to handle twice as many hash collisions as a single-level H-CAM (e.g., FIG. 6). Rather, it is the ability to do such with appreciably less circuit elements (and thus also less cost, footprint, and power consumption). A four-level H-CAM (e.g., FIG. 5) has a similarly nonlinear ability.

Regarding claims 19-26, generally, we urge that these are allowable for at least the reasons stated above.

Item 5 (Conclusion):

This appears informational in nature and is understood to require no reply.

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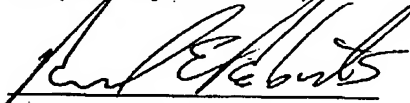
CONCLUSION

Applicant has endeavored to put this case into complete condition for allowance. It is thought that the objections and §112 rejections have all been corrected by amendment or have been completely rebutted, and the §102 rejections and the §103 rejections have been shown to be unfounded on the prior art reference cited. Applicant therefore asks that all objections and rejections now be withdrawn and that allowance of all claims presently in the case be granted.

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